DFEB2

Digital Front End
Run IIB Upgrade

Custom Backplane Specification

DØ Note 4674
Engineering Note 2004-02-05a

APPROVED FOR PRODUCTION

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1 Overview

This is a standard VME size, 21 slot, 6U monolithic backplane with custom connectors in all slots. Hard Metric connectors will be used on all slots, and in this document ERNI part numbers are referenced. 48VDC power distribution will be used on this backplane, thus eliminating the need for high current bus bars. None of the boards will be hot swappable, thus all of the pins can be the same length. The total thickness of the backplane should be at least 3.2mm (0.125") to insure mechanical stability.

A crate controller (DFEC2) resides in slot 1 of this crate. Slots 2 through 21 will contain DFEA2 boards. The DFEC2 will communicate over a 16-bit address 16-bit data bus to all DFEA2 boards. This propriateary address/data bus is similar to VME, but has fewer control signals. The DFEC2 also distributes a 53MHz clock and associated control bits to all DFEA2 boards.

DFEA2 boards are primarily pass through boards – that is, there is not much information that must be shared between DFEA2 boards. Most of the high speed communication occurs over point-to-point Low-Voltage Differential Signal (LVDS) channel link cables which plug into the rear of the backplane.

2 DFEA2 Boards [slots 2-21]

For DFEA2 The backplane will support up to ten input cables and four output cables passing through the backplane A and B connectors and onto the DFEA2 boards. In addition, up to six coaxial connectors will pass through a type L hard metric connector and onto cables plugged into the rear of the backplane.

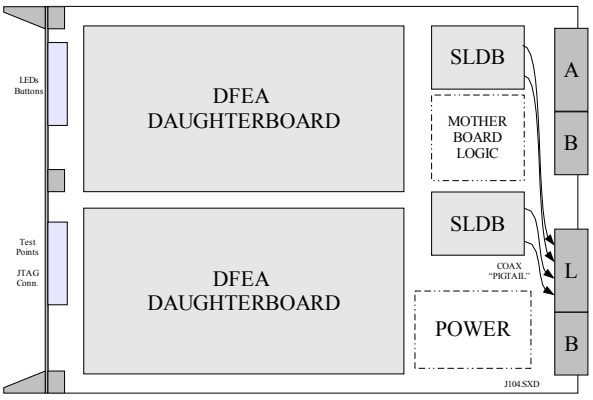


Figure 1: An example of a DFEA2 board. Coaxial cable pigtails connect to Serial Link Daughterboards (SLDBs).

2.1 Board Mechanical Drawing

A drawing of the DFEA2 board showing connector locations is available in [PDF] or AutoCad [DWG] format on the DFE Upgrade Hardware webpage [1].

2.2 Board Pinout

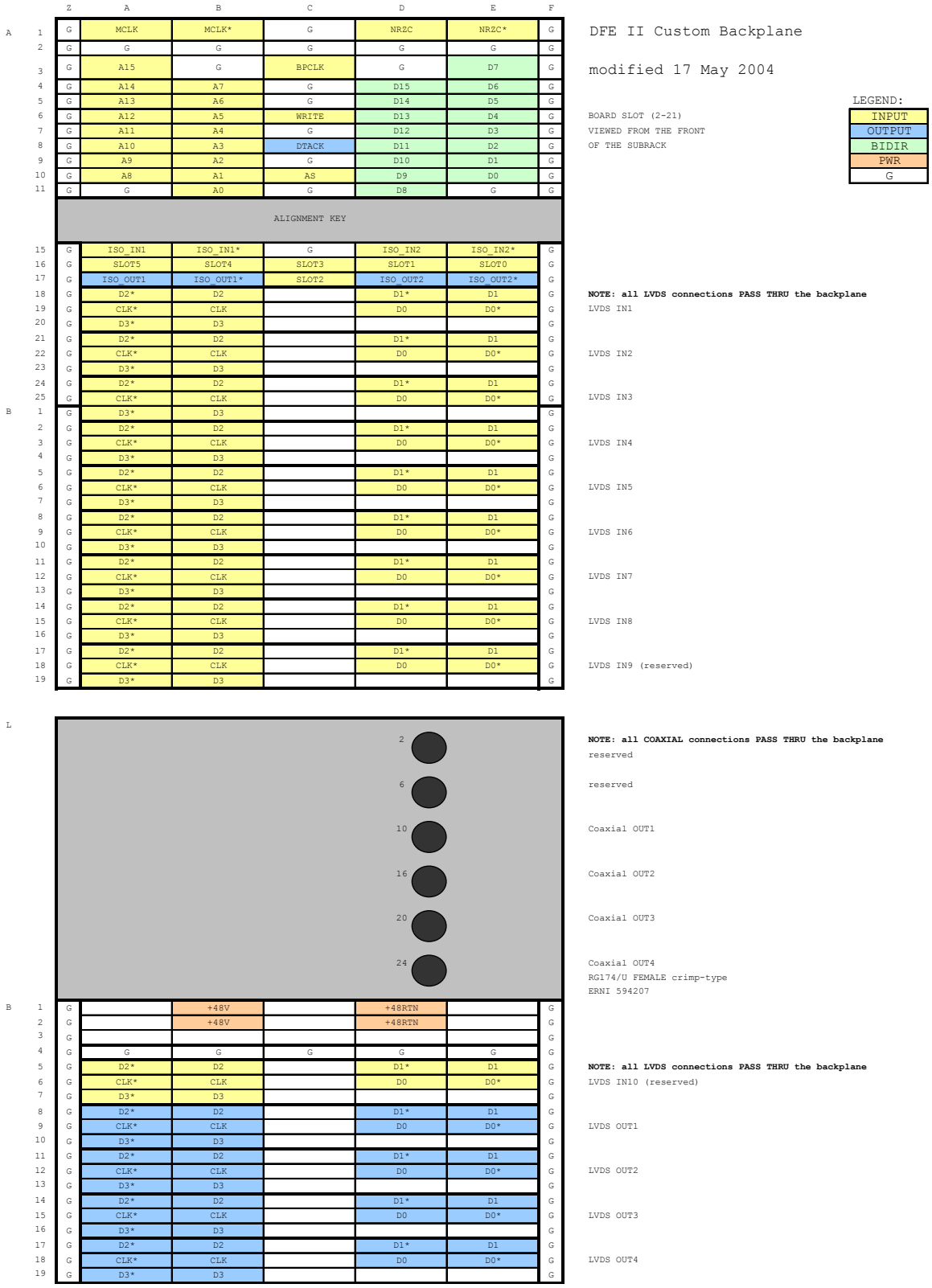


Figure 2: DFEA2 board backplane pinout (slots 2-21), *as viewed from the front of the crate.* Note that the LVDS and Coaxial connections pass through the backplane.

2.3 LVDS Cables

Each LVDS cable consists of six twisted pairs (five are used) which terminate in a 5x3 hard metric connector body. The cables used in this application are AMP/TYCO part number 621409-X which are designed to plug into hard metric connectors

The type A and B hard metric connectors in slots 2-21 will pass through the backplane, and shrouds will be installed on the rear of the backplane. Retaining clips will hold the cables into these shrouds (the cable retaining clips will be supplied by and installed at Fermilab). The pin length in the front (Male Connector) should be 5.2mm ("Level 1"). Assuming the backplane thickness (Y) is ~3.2mm, pin lengths and shroud base thickness (H) should be selected so that the pin length on the backside is at least 5mm to insure proper mating to the LVDS cables.

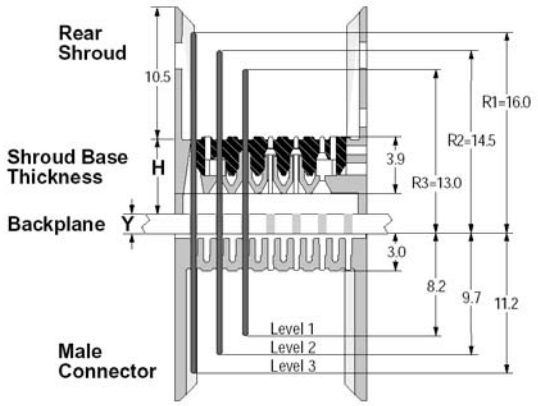


Figure 3: Cross section view of the backplane and hard metric connectors.

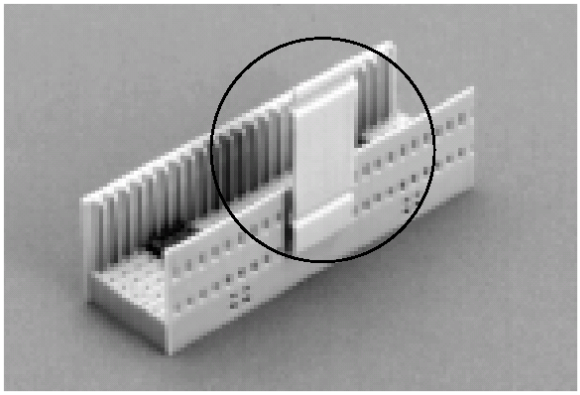


Figure 4: LVDS cable retaining clip on the shroud.

2.4 Coaxial Cabling

A hard metric type L connector is used to pass coaxial connections through the backplane. The DFEA2 board will use a type L connector (ERNI 044579) body with up to six RG174/U male coaxial connectors (ERNI 594213). The backplane will use a mating connector body (ERNI 104146) which will hold up to six RG174/U female connectors (ERNI 594207) which will be crimped onto coaxial cables.

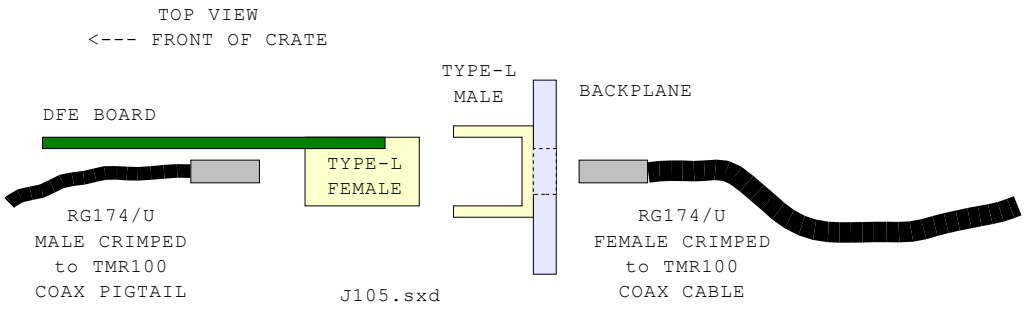


Figure 5: Coaxial cable connection through the backplane.

Note that the RG174/U connectors can be crimped onto the existing coaxial cables and snapped into the type L connector bodies at any time.

3 DFEC2 Crate Controller [slot 1]

The DFEC2 resides in slot 1 of the crate. This controller is the master of a simple, synchronous, proprietary A16 D16 data bus; it is also responsible for receiving timing and control signals and distributing them over the backplane to slots 2-21.

The slot 1 connector consists of a type A and type B hard metric connector. Note: the pinout of the type A hard metric connector is backward compatible with legacy DFE hardware. The type A and B hard metric connectors used in this slot do not pass through, so no shrouds are needed on the backside of the backplane. The pin length should be 5.2mm ("Level 1") for both connectors.

3.1 Board Mechanical Drawing

A drawing of the DFEC2 board showing connector locations is available in [PDF] or AutoCad [DWG] format on the DFE Upgrade Hardware webpage [1].

3.2 Backplane Pinout

		Z	A	B	C	D	E	F
A	1	G	G	D4	G			G
	2	G	D3	D5	G	G	G	G
	3	G	D2	G	D0	D1	G	G
	4	G		D6		D7	BPCLK	G
	5	G			G		WRITE	G
	6	G				G		G
	7	G		A8				G
	8	G		A15		A7	G	G
	9	G	A14	A6	A13	A5	A12	G
	10	G	A4		A11	G	G	G
	11	G	A3	A10	A2	A9	G	G
		ALIGNMENT KEY						
	15	G		A1		A8	DTACK	G
	16	G	A0	G		G	G	G
	17	G	G		G	G		G
	18	G	G	G	G	G		G
	19	G	G		G		G	G
	20	G		G		G		G
	21	G			G		G	G
	22	G						G
	23	G						G
	24	G						G
	25	G						G
B	1	G	NRZC_1*	G	MCLK_4	G	D15	G
	2	G	NRZC_1	G	MCLK_4*	G	G	G
	3	G	G	NRZC_3	G	G	D14	G
	4	G	G	NRZC_3*	G	G	G	G
	5	G	MCLK_1	G	NRZC_5	G	D13	G
	6	G	MCLK_1*	G	NRZC_5*	G	G	G
	7	G	G	MCLK_3	G	G	D12	G
	8	G	G	MCLK_3*	G	G	G	G
	9	G	NRZC_2*	G	MCLK_5	G	D11	G
	10	G	NRZC_2	G	MCLK_5*	G	G	G
	11	G	G	NRZC_4	G	G	D10	G
	12	G	G	NRZC_4*	G	G	G	G
	13	G	MCLK_2	G	G	G	D9	G
	14	G	MCLK_2*	G	G	G	G	G
	15	G	G	G	G	G	D8	G
	16	G						G
	17	G						G
	18	G		+48V		+48RTN		G
	19	G		+48V		+48RTN		G

INPUT
OUTPUT
BIDIR
PWR
G — Ground
No Connection

Figure 6: Slot 1 backplane pinout, as viewed from the front of the crate.

4 Backplane Signal Distribution

4.1 Read/Write Bus

The following single-ended signals are driven by the controller in slot 1 and are bussed to slots 2 thorough 21.

Table 1: Terminations for the Read/Write Bus lines.

PIN	DESCRIPTION	TERMINATION
A15-A0	address bus	100 ohm pulldown
D15-D0	bidirectional data bus	100 ohm pulldown
BPCLK	~7.5MHz clock	100 ohm pulldown
WRITE	write enable	100 ohm pulldown
AS	address strobe	100 ohm pulldown
DTACK	data acknowledge	

All of these backplane signals should be considered high speed signals and care should be taken to minimize crosstalk. A single ended impedance of 100 ohms should be maintained on the BPCLK line. Termination resistors should be located near slot 21 and they should be accessible from the rear of the crate. Socketed “isolated” type SIP resistor networks are preferred.

4.2 Slot ID pins

Slots 2 through 21 have six pins used for slot identification, these pins are called slot[5..0]. The slot[4..0] pins will encode the slot number: 2 (00010) to 21 (10101). The slot[5] signal is common to slots 2 through 21; its value will be determined using a jumper or dip switch accessible from the back of the crate. Each slot pin will either be tied to ground (logic 0) or left unconnected (logic 1).

4.3 Master Clock and Control Bit Distribution

The DFEC2 distributes clock and control bits to the boards in slots 2 through 21. This information is sent over two differential pairs: MCLK/MCLK* is the 53MHz clock; and NRZC/NRZC* are the system control bits. These signals are differential pairs and should be routed to maintain 100Ω differential impedance.

In order to minimize capacitive loading and control skew the crate controller drives five copies of these signals. Each signal touches four slots and then ***terminates on the backplane***. For example, the MCLK_1/MCLK_1* signal is shown below:

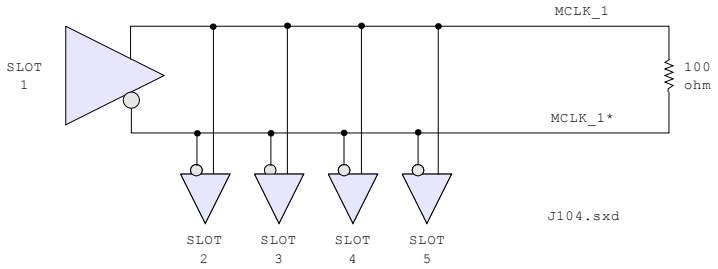


Figure 7: Backplane clock distribution to groups of four slots.

Likewise, the NRZC_1/NRZC_1* pair also goes to slots 2-5; MCLK_2/MCLK_2* and NRZC_2/NRZC_2* go to slots 6-9, etc. as shown below:

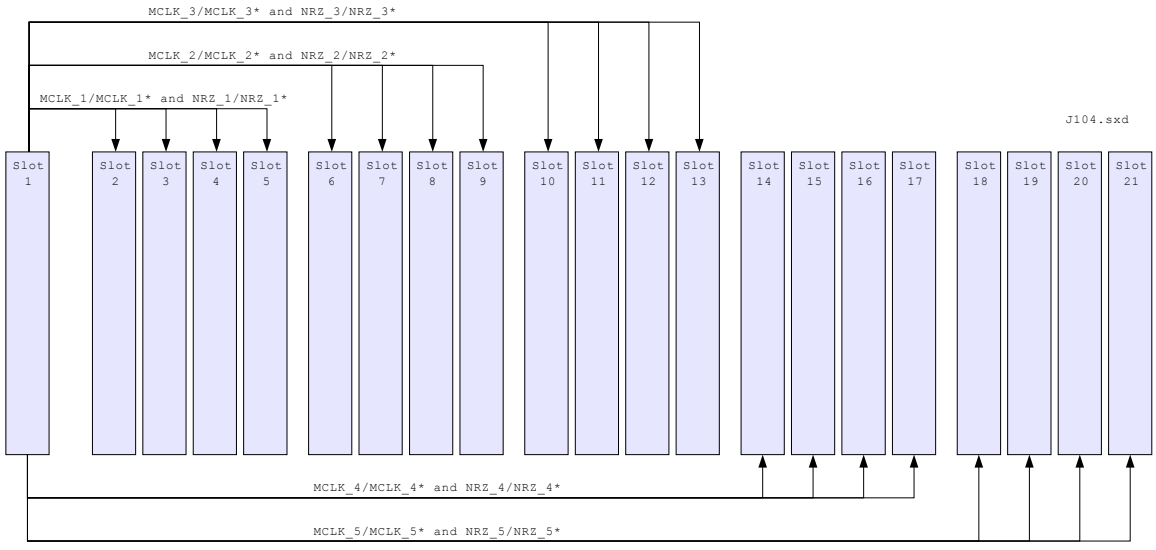


Figure 8: Master Clock and Control Bit Distribution

The termination resistor should be located on the backplane near the last slot in the sequence.

4.4 Isolated Track Bits

The boards in slots 2 through 21 need to share data with their neighboring boards over dedicated differential pairs as shown below:

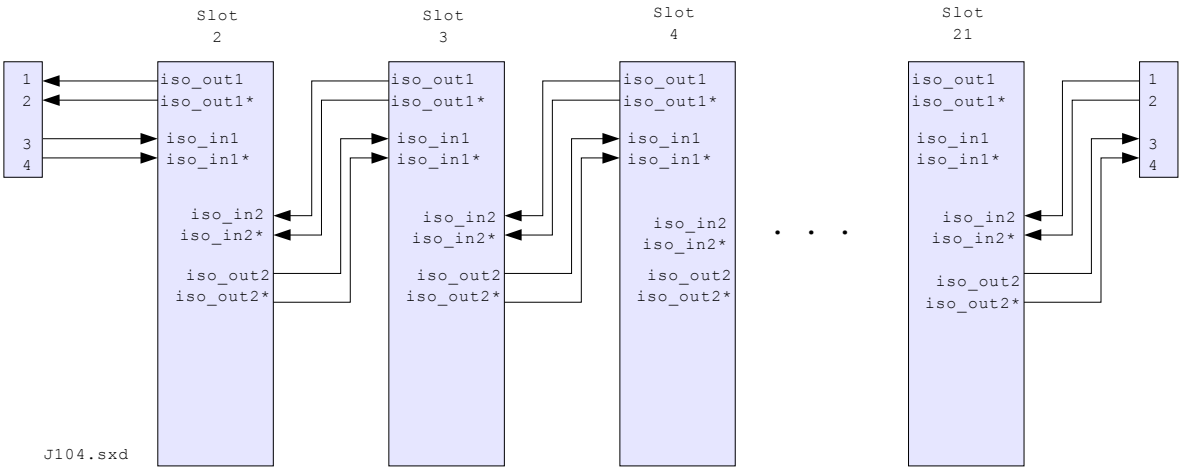


Figure 9: Isolated Track nets between backplane slots.

Slots 2 and 21 have connectors which allow cables to send this information between crates. These backplane connectors should be ten pin 0.100" IDC type with latches (AMP 499910-1 or equivalent). The iso_out/iso_out* and iso_in/iso_in* signals should be routed as 100Ω differential pairs on the backplane.

5 Power Distribution

The backplane will distribute +48V to all boards. Each board in the crate will use an isolated DC-DC converter and switching regulator to produce the required supply voltages needed for operation. This power distribution scheme provides good voltage regulation on the board while eliminating heavy cables, remote sensing oscillations, and potentially dangerous low-voltage high current supplies.

5.1 Bulk Supply to Backplane

A bulk 48VDC supply will supply power to the backplane using a pair of 8AWG cables. These cables will be fused at **20A** near the bulk supply. The backplane will require good solid (bolt type) connections: +48VDC, +48VDC_RETURN, and GROUND. An ERNI Power Tap type connection is shown below:

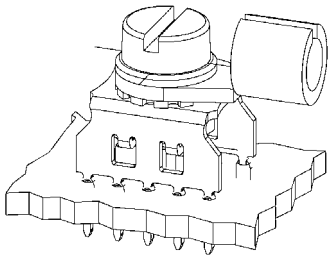


Figure 10: An example power terminal for the backplane.

The backplane GROUND connection should have a very low impedance; a minimum of 3 power taps should be used for the ground connection. A minimum of two power taps should be used for each +48VDC and +48VDC_RETURN connection.

5.1.1 Remote Sense Connector

A three position terminal block header (Phoenix Contact 1803439 or equivalent) shall be installed on the rear of the backplane. The three pins should be connected to +48VDC, +48VDC_RETURN, and GROUND. The +48VDC and +48VDC_RETURN connections should be fused with a 2A fast-acting fuse (Cooper Bussman TR/SFT-2 or equivalent).

5.2 Backplane to Boards

Using 48VDC distribution eliminates high currents anywhere in the system, so large bus bars are not needed. Thus the 48VDC can be distributed through the backplane using power planes or copper pours. For each backplane slot two pins will be used for +48V and another pair of pins will be used for the +48V return. The top (and bottom) shields on the hard metric connectors will be used for a ground connection. Additionally, there are ground pins scattered throughout the hard metric connectors as well.

5.2.1 Fusing

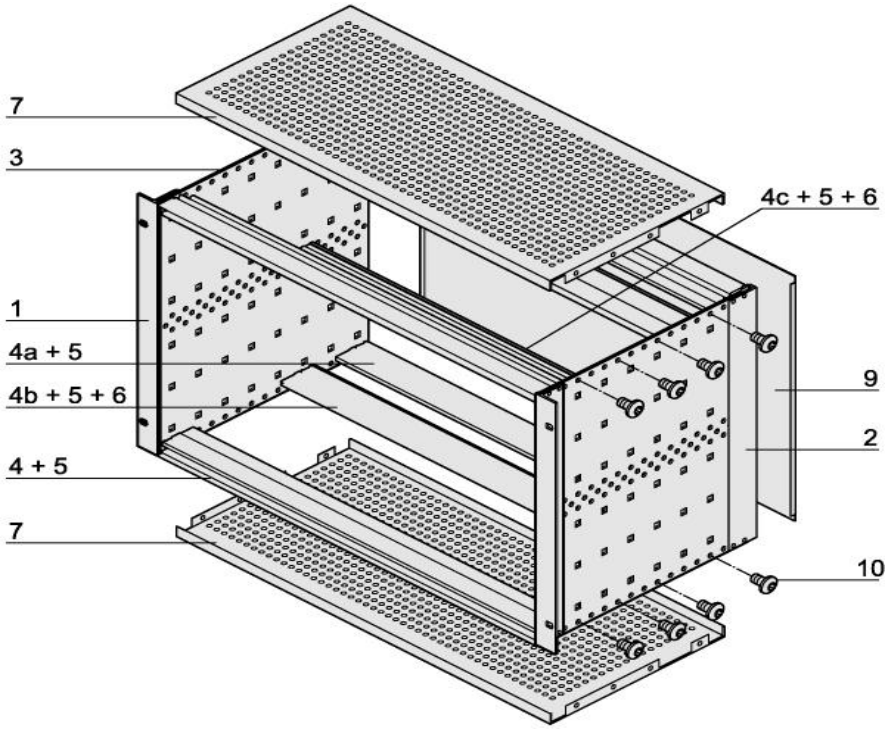
Each slot in the backplane will be protected by a 2A fast-acting fuse (Cooper Bussman TR/SFT-2 or equivalent). These fuses shall be installed between the +48V plane and the +48V pins on each connector. These surface mount fuses should be accessable from the rear of the backplane.

5.3 Power Supply Filtering

The vendor will provide locations on the backplane where capacitors may be installed to provide additional filtering. *These capacitors will be supplied by and installed at Fermilab as necessary.* Evenly space footprints for five electrolytic capactors (Panasonic ECA-2AM102) on the backplane.

6 Crate Mechanical

The DFE crate is a standard 6U x 370mm HF VME-type subrack. The cover plates (7) will be installed, however the back (9) will not be installed. The from rails (4) and perforated strip (5) should be compatible with HL (high leverage) type handles. A center horizontal rail (4c) will not be used, so the backplane must be thick enough to withstand board insertion forces without flexing.



The following part numbers are for Schroff hardware.

item	quantity	description	number
3	2	side panel 6Ux370mm	30838-976
1	2	mounting angle for 19" subrack	30847-815
4	2	front rail for HL handles	30846-465
4A	2	rear rail for backplanes	30819-241
2	2	rear trim	30847-830
6	2	perforated strip for HF handles	30845-253
7	2	cover plates	30845-567
	42	card guides for 320mm cards	custom???

7 References

1. DFE Upgrade Hardware Webpage
http://www-d0.fnal.gov/~jamieson/run2b

8 Revision History

05 Feb 2004: First Draft

25 Feb 2004: Minor changes to overview, removed figure from section 5. Added crate mechanical section. Misc. cosmetic stuff.

05 Mar 2004: Moved backplane connectors on the DFE boards to provide more space for LVDS routing. Change to the DFE board connector pinout!

22 Apr 2004: FINAL DRAFT APPROVED FOR PRODUCTION. Modified section 2.3: the retaining clips will be supplied by and installed at Fermilab. Added section 5.3, which specifies filter capactor footprints. Added section 5.2.1, which specifies fuses for each slot. Modified section 5.1, specify the minimum number of power taps for +48VDC, +48VDC_RETURN, and GROUND. Added section 5.1.1. remote sense connector.

18 May 2004: Changed the backplane pinout *(again!)* for slots 2-21. The +48V and +48VRTN power pins moved down to the bottom connector, and all of the LVDS inputs moved up three rows.

06 Jan 2005: Purely cosmetic changes on the board names. now using DFEB2, DFEC2, and DFEA2 to refer to the new hardware. No technical specification changes in this version. Make it a d0 note.